AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior version, and listings, of claims in the application:

Listing of Claims

Claim 1 (Currently Amended): A multilayer printed circuit board comprising a plurality of interlaminar insulating layers and conductor circuits, said printed circuit board being formed by laminating a first interlaminar insulating layer on a conductor circuit of a substrate and forming at least a second conductor circuit and a second interlaminar insulating layer on the first interlaminar insulating layer, wherein the conductor ~~circuit is~~ circuits are comprised of an electroless plated film and an electrolytic plated film, and a roughened layer formed by a roughening treatment on at least a part of the surface of the conductor ~~circuit~~ circuits.

Claim 2 (Currently Amended): A multilayer printed circuit board comprising a plurality of interlaminar insulating layers and conductor circuits, said printed circuit board being formed by laminating a first interlaminar insulating layer on a conductor circuit of a substrate and forming at least a second conductor circuit and a second interlaminar insulating layer on the first interlaminar insulating layer, wherein the conductor ~~circuit is~~ circuits are comprised of an electroless plated film and an electrolytic plated film, and a roughened layer formed by a roughening treatment on at least a part of the surface of the conductor ~~circuit~~ circuits, and the surface of the roughened layer is covered with a layer of a metal having an ionization tendency of more than copper but not higher than titanium, or of a noble metal.

Claim 3 (Previously Presented): A printed circuit board according to claim 1, wherein the

roughened layer is on at least a part of the surface inclusive of a side surface of the conductor circuit.

Claim 4 (Previously Presented): A printed circuit board according to claim 1, wherein the roughened layer is on at least a part of a side face of the conductor circuit.

Claim 5 (Previously Presented): A printed circuit board according to claim 1, wherein the roughened layer is a plated layer of copper-nickel-phosphorus alloy.

Claim 6 (Previously Presented): A method of producing a multilayer printed circuit board comprising subjecting a surface of a substrate to an electroless plating, forming a plating resist thereon, subjecting the substrate to an electrolytic plating, removing the plating resist, etching and removing the electroless plated film beneath the plating resist to form a conductor circuit comprised of the electroless plated film and the electrolytic plated film, forming a roughened layer on at least a part of the surface of the conductor circuit and then forming an interlaminar insulating layer.

Claim 7 (Previously Presented): A method of producing a multilayer printed circuit board comprising subjecting a surface of a substrate to an electroless plating, forming a plating resist thereon, subjecting the substrate to an electrolytic plating, removing the plating resist, etching and removing the electroless plated film beneath the plating resist to form a conductor circuit comprised of the electroless plated film and the electrolytic plated film, forming a roughened layer on at least a part of the surface of the conductor circuit, covering the surface of the roughened layer with a layer of a metal having an ionization tendency of more than copper but not higher than titanium, or of a noble metal, and forming an interlaminar insulating layer.

Claim 8 (Previously Presented): A method of producing a printed circuit board according to claim 6, wherein the roughened layer is formed by plating of copper-nickel-phosphorus alloy.

Claim 9 (Currently Amended): A multilayer printed circuit board comprising a substrate provided with an under layer conductor circuit, an interlaminar insulating layer formed thereon and an upper layer conductor circuit formed on the interlaminar insulating layer, and a viahole connecting both the conductor circuits to each other, in which the viahole is comprised of an electroless plated film and an electrolytic plated film, and a roughened layer on at least a part of the surface of the under layer conductor circuit connected to the viahole, said roughened layer having a roughened surface formed by etching treatment, polishing treatment, ~~or~~ redox treatment or plating treatment ~~, or having a roughened surface formed by a plated film on at least a part of the surface of the underlayer conductor circuit connected to the viahole~~.

Claim 10 (Original): A multilayer printed circuit board according to claim 9, wherein the roughened layer is formed by plating of copper-nickel-phosphorus alloy.

Claim 11 (Previously Presented): A method of producing a multilayer printed circuit board comprising forming a lower conductor circuit layer on a surface of a substrate, forming a roughened layer by etching treatment, polishing treatment, redox treatment, or plating treatment on at least a part of the surface of the underlayer conductor circuit connected to a viahole, forming an interlaminar insulating layer thereon, forming openings for viaholes in the interlaminar insulating layer, subjecting the interlaminar insulating layer to an electroless plating, forming a plating resist thereon, subjecting the interlaminar insulating layer to an electrolytic plating, removing the plating resist, etching and removing the electroless plated film beneath the plating resist to form an

upperlayer conductor circuit comprised of the electroless plated film and the electrolytic plated film and a viahole.

Claim 12 (Original): A method of producing a multilayer printed circuit board according to claim 11, wherein the roughened layer is formed by plating of copper-nickel-phosphorus alloy.

Claims 13-21 (Canceled)

Claim 22 (Previously Presented): A printed circuit board according to claim 2, wherein the roughened layer is on at least a part of the surface inclusive of a side surface of the conductor circuit.

Claim 23 (Previously Presented): A printed circuit board according to claim 2, wherein the roughened layer is on at least a part of a side face of the conductor circuit.

Claim 24 (Previously Presented): A printed circuit board according to claim 2, wherein the roughened layer is a plated layer of copper-nickel-phosphorus alloy.

Claim 25 (Previously Presented): A printed circuit board according to claim 3, wherein the roughened layer is a plated layer of copper-nickel-phosphorus alloy.

Claim 26 (Previously Presented): A printed circuit board according to claim 4, wherein the roughened layer is a plated layer of copper-nickel-phosphorus alloy.

Claim 27 (Previously Presented): A method of producing a printed circuit board according to claim 7, wherein the roughened layer is formed by plating of copper-nickel-phosphorus alloy.

Claims 28-43 (Canceled)

Claim 44 (Previously Presented): The printed circuit board according to claim 1, wherein the electrolytic plated film is formed on the electroless plated film.

Claim 45 (Previously Presented): The printed circuit board according to claim 2, wherein the electrolytic plated film is formed on the electroless plated film.

Claim 46 (Previously Presented): The method according to claim 6, wherein the electrolytic film is formed on the electroless plated film.

Claim 47 (Previously Presented): The method according to claim 7, wherein the electrolytic film is formed on the electroless plated film.

Claim 48 (Previously Presented): The printed circuit board according to claim 9, wherein the electrolytic film is formed on the electroless plated film.

Claim 49 (Previously Presented): The method according to claim 11, wherein the electrolytic film is formed on the electroless plated film.

Claim 50 (New) A printed circuit board according to claim 1, wherein the roughening treatment comprises etching treatment, polishing treatment, redox treatment, or plating treatment.

Claim 51 (New) A printed circuit board according to claim 2, wherein the roughening treatment comprises etching treatment, polishing treatment, redox treatment, or plating treatment.

Claim 52 (New) A printed circuit board according to claim 1, wherein the electroless plated film comprises an inner layer side and the electrolytic plated film comprises an outer layer side and the roughened layer is formed on the electrolytic plated film.

Claim 53 (New) A printed circuit board according to claim 2, wherein the electroless plated film comprises an inner layer side and the electrolytic plated film comprises an outer layer side and the roughened layer is formed on the electrolytic plated film.

Claim 54 (New) A printed circuit board according to claim 9, wherein the electroless plated film comprises an inner layer side and the electrolytic plated film comprises an outer layer side and the roughened layer is formed on the electrolytic plated film.